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Effect of copper interlayer on thermally deposited polycrystalline Ge-thin film transistors fabricated on glass substrates

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Abstract : Here we reported the performance of Ge- thin film transistors (TFTs) with a copper interlayer in the channel region. All the TFTs are fabricated in staggered electrode structure on perfectly cleaned glass substrates using thermal evaporation process. Rare earth oxide Dy_2O_3 is used as gate insulator. The TFTs are annealed at 370°C at high vacuum. The TFT exhibits a better mobility of 0.646 $cm^2V^{-1}s^{-1}$, than the TFT, fabricated without copper interlayer, mobility of which is found as 1.44×10^{-3} $cm^2V^{-1}s^{-1}$. The characteristics and some electrical parameters of the TFTs with copper interlayer are evaluated and compared with that of TFTs fabricated without copper interlayer.

Keywords : Poly Ge-TFT, copper interlayer, Dy_2O_3, mobility.

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1. Introduction

In the recent years, TFTs are widely used as driving devices in large area electronics circuits. Particularly in active matrix liquid crystal displays (AMLDs), TFTs are used as pixel transistors [1]. The passivation of grain boundary states by atomic hydrogen is a well-established technique to reduce the grain boundary potential barrier in poly-Si [2]. An enlargement of the grain size and a reduction of the barrier height at the grain boundaries by means of hydrogen passivation have been investigated in order to improve the carrier mobility in poly-Si TFTs [3]. It has been reported that, copper passivation of dislocation in polycrystalline silicon reduces the potential barrier height at the grain boundaries [4].

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Many investigators [5-7] have shown that rare earth oxides play an important role in thin film transistors as gate insulators due to their high chemical stability, high dielectric constant and high resistivity.

In this investigation we have reported the performance of poly Ge-TFTs with copper interlayer fabricated on glass substrates with Dy_2O_3 as gate insulator. Also the characteristics of the TFTs with copper interlayer are compared with the TFTs fabricated without copper interlayer.

2. Experimental details

In this investigation the TFTs were fabricated using thermal evaporation process in high vacuum better than $4x10^{-6}$ torr. All the TFTs were deposited in staggered electrode structure on glass substrates. Aluminium was deposited first as source-drain electrodes. A channel of 50-μm lengths was produced with the help of a wire grill, fixed on the mask. A 1055 Å channel layer was formed between the source-drain gap by deposition of Ge (512 Å), Cu (23 Å) and Ge (520 Å) layers in steps. The Ge/Cu/Ge layers are deposited at substrate temperature of 250°C with a deposition rate of 0.5 $Å s^{-1}$. A layer of Dy_2O_3 of thickness 715 Å was deposited as gate insulator over the Ge/Cu/Ge layers. Finally, a layer of Al was deposited on the oxide layer as gate electrode. The fabricated TFTs were annealed in high vacuum at 370°C for 5 to 6 hours. Figure 1 shows a schematic structure of the TFT with a copper interlayer.

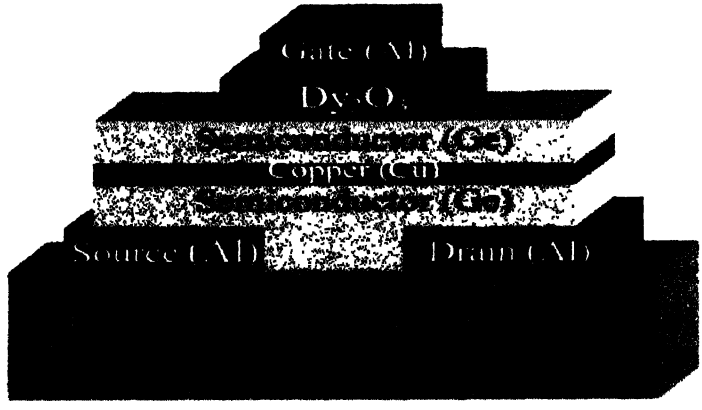

Figure 1. Schematic diagram of the staggered electrode structure of the TFT fabricated with a copper interlayer.

Ge- Dy_2O_3 TFTs without copper interlayer have also been fabricated with the similar procedure as mentioned above. These TFTs are also annealed to a temperature of 370°C for 5 to 6 hours.

The film thicknesses were measured by multiple beam interference method. The gate capacitance was measured using auto computer LCR sortester (APLAB, Model 4912). The drain current, drain voltage and gate voltage were measured using the digital nanoammeters and digital multimeters.

3. Results and discussions

3.1. Electrical characteristics of the TFTs :

Well-modulated drain current (I_d) *vs.* drain voltage (V_d) characteristics of the TFTs, with a copper interlayer with constant gate voltages (V_g) have been observed which are shown in Figure 2. Figure 3 shows the typical drain current (I_d) *vs* gate voltage (V_g) curve for the TFT at drain voltage V_d = 8V.

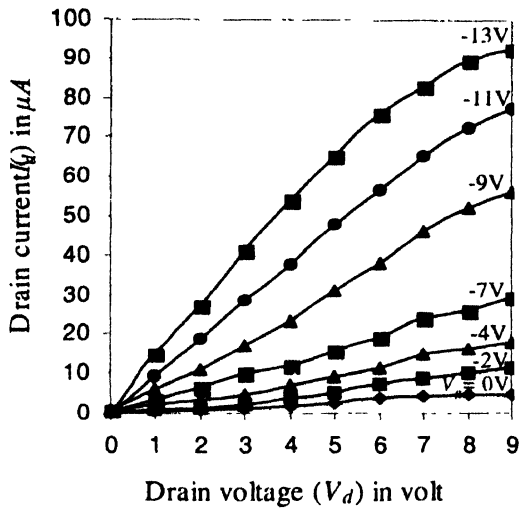

Figure 2. I_d – V_d curves of the TFT's with copper interlayer.

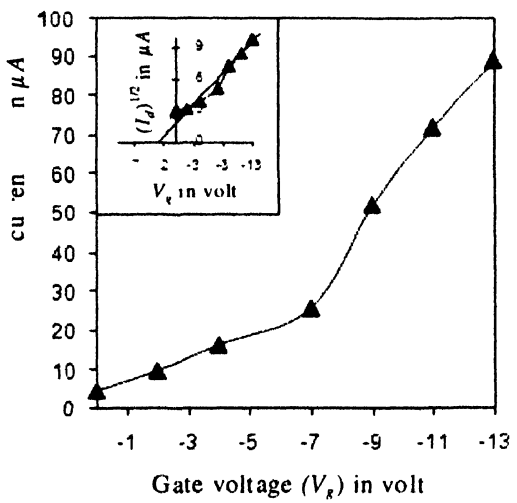

Figure 3. I_d - V_g curves of the TFT's with copper interlayer. The inset shows variation of $\sqrt{I_d}$ at different V_g

The transconductance (g_m) of the devices is estimated from the eq. (1) given by [8]

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d=const.} = \mu_{FET} C_{ox} \frac{V_d}{l^2} \qquad (1)$$

where C_{ox} is the gate capacitance per unit area, l is the channel length, V_d is the drain voltage and μ_{FET} is the field effect mobility.

The electrical parameters of TFTs can be calculated using the following expressions: output drain resistance

$$r_d = \left.\frac{\delta V_d}{\delta I_d}\right|_{Vg=const} \qquad (2)$$

amplification factor

$$\mu = g_m \times r_d \qquad (3)$$

and gain-bandwidth (*G.Bw*) product

$$G.Bw = \frac{g_m}{2\pi C_{rr}} \tag{4}$$

From eq. (1), the mobility μ_{FET} can be estimated. The calculated values of output drain resistance (r_d), transconductance (g_m), amplification factor (μ), mobility μ_{FET} and the gain-bandwidth product (*G.Bw*) of the TFTs are presented in Table 1.

3.2. Comparison with TFTs fabricated without copper interlayer:

The characteristics and the calculated parameters of the TFTs fabricated with copper interlayer are compared with that of the TFTs fabricated without copper interlayer. The drain current (I_d) *vs.* drain voltage (V_d) characteristics of the TFTs, without copper interlayer are shown in Figure 4. It is apparent from Figures 2 and 4 that the family of drain current of the TFTs with copper interlayer exhibits higher drain current than the TFTs without copper interlayer. This is due to their higher mobility and lower threshold voltage (V_T).

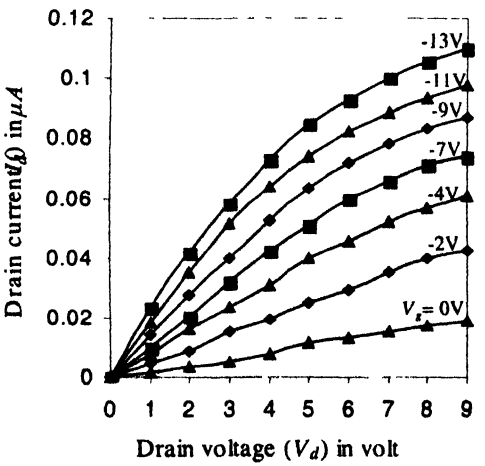

Figure 4. I_d – V_d curves of the TFT's without copper interlayer.

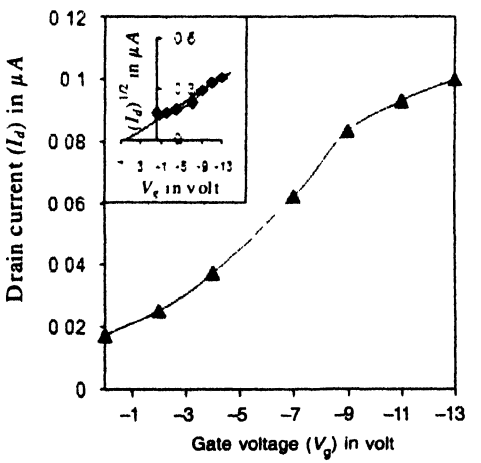

Figure 5. I_d - V_g curves of the TFT's without copper interlayer. The inset shows variation of $\sqrt{I_d}$ at different V_g

Figure 5 shows the drain current (I_d) *vs.* gate voltage (V_g) curve at drain voltage V_d = 8V for the TFT without copper interlayer. The threshold voltage (V_T) of the TFTs with copper interlayer and without interlayer have been evaluated by plotting $\sqrt{I_d}$ *vs.* gate voltage (V_g) at constant drain voltage (V_d), which are shown in the inset of Figures 3 and 5 respectively. In the inset of Figures 3 and 5, a straight line is drawn through the linear region of the $\sqrt{I_d}$ *vs.* gate voltage (V_g) curves. From the intercepts with the horizontal axis, the threshold voltages (V_T) of the TFTs with copper interlayer and without copper interlayer are determined and these are noted as 3V and 6.4V respectively. The estimated values of

the electrical parameters of the TFTs without copper interlayer are also presented in Table1. Using eq. (1), the mobilities are estimated and found as 0.646 $cmV^{-1}s^{-1}$ for TFTs with copper interlayer and $0.4x10^{-3}$ for TFTs without copper interlayer. The enhance mobility of the TFT's with copper interlayer can be explained as follows. In this investigation we may say that, during the heat treatment, the grain boundary states in the case of poly- Ge TFTs are passivated by copper in Ge. During the passivation, copper atom diffuses along the grain boundaries and completes some of the opened bonds (dangling bonds). Consequently the interface states density drops and the potential barrier is lowered. The resulting effect is that the poly-Ge electrically progresses towards single crystal Ge characteristics, yielding higher mobility.

The gain-bandwidth products of the devices are found very low. The gain- bandwidth product depends on mobility and is a function of the channel length. Improvement in the gain-bandwidth product can be accomplished by reducing the channel length. An attempt to use too small a channel length will give trouble if the resulting gap region is not sharply defined. Hence to get the high value of gain-bandwidth product, the mobility of the carrier must be increased [8]. In this investigation, the TFTs exhibit low mobility, hence the devices exhibit low gain-bandwidth product.

Table 1. Comparison of some parameters of the TFTs with copper interlayer and without copper interlayer.

Type of TFTs	Output resistance r_d (ohm)	Transconductance g_m (mho)	Amplification factor μ	Mobility μ_{FET} ($cm^2V^{-1}s^{-1}$)	Gain bandwidth product $G.Bw$ (KHz)
with Copper interlayer	0.125×10^6	3.86×10^{-6}	0.49	0.646	1.31×10^{-2}
without copper interlayer	89.29×10^6	0.0083×10^{-6}	0.70	1.44×10^{-3}	29.35×10^{-2}

4. Conclusion

TFTs with copper interlayer exhibit a higher mobility than the TFTs without copper interlayer. It is observed that the threshold voltage (V_T) is significantly improved in case of TFTs with copper interlayer. The other electrical properties such as output resistance (r_d) and transconductance (g_m) are also found better in case of TFTs with copper interlayer, but amplification factors (μ) are comparable for both types of TFTs. From this observation it may also be concluded that the rare earth oxide Dy_2O_3 can be used as a dielectric layer in TFTs.

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